UM1575
User manual

Spice model tutorial for Power MOSFETs

Introduction

This document describes ST's Spice model versions available for Power MOSFETs. This is a guide designed to support user choosing the best model for his goals. In fact, it explains the features of different model versions both in terms of static and dynamic characteristics and simulation performance, in order to find the right compromise between the computation time and accuracy. For example, the self-heating model (V3 version), which accurately reproduces the thermal response of all electrical parameters, requires a considerable simulation effort.

Finally, an example shows how the self-heating model works.

Spice models describe the characteristics of typical devices and don't guarantee the absolute representation of product specifications and operating characteristics; the datasheet is the only document providing product specifications.

Although simulation is a very important tool to evaluate the device's performance, the exact device's behavior in all situations is not predictable, therefore the final laboratory test is necessary.

1 Spice model versions

ST provides 6 model versions on each part number:

- partnumber_V1C
- partnumber_V1T
- partnumber_V2
- partnumber_V3
- partnumber_V4
- partnumber_TN

V1C version

It is the basic model (LEVEL =3) enclosing C_{oss} and C_{rss} modeling through capacitance profile tables. It is an empirical model, and it assumes a 27 °C constant temperature.

V1T version

It comes directly from V1C version and it also includes the package thermal modeling through a thermal equivalent network and presents two additional external thermal nodes T_j and T_{case}. This version hasn't the dynamic link between Power MOSFET temperature and internal parameters.

V2 version

It is more advanced than V1C, in fact it takes into account the temperature dependence and capacitance profiles too. It allows the static and dynamic behavior to be reproduced by user at fixed temperatures. By using this version, the simulation of self-heating effects isn't possible.

V3 version

It comes directly from V2 version and includes the package thermal model through a thermal equivalent network and presents two additional external thermal nodes: T_j and T_{case}. In this version, during each transient, the current power dissipation is calculated and a current proportional to this power is fed into the thermal network. In this way, the voltage at T_j node contains all the information about the junction temperature, which changes internal device's parameters. Since it is a monitoring node, usually T_j pin is not connected (however, to avoid warning messages on this node, the user has to add a floating wire - see *Figure 1*). On contrary, T_{case} node has to be connected, either to a constant voltage source Vdc representing the ambient temperature or to a heat sink modeled by its own thermal network (*Figure 1*).

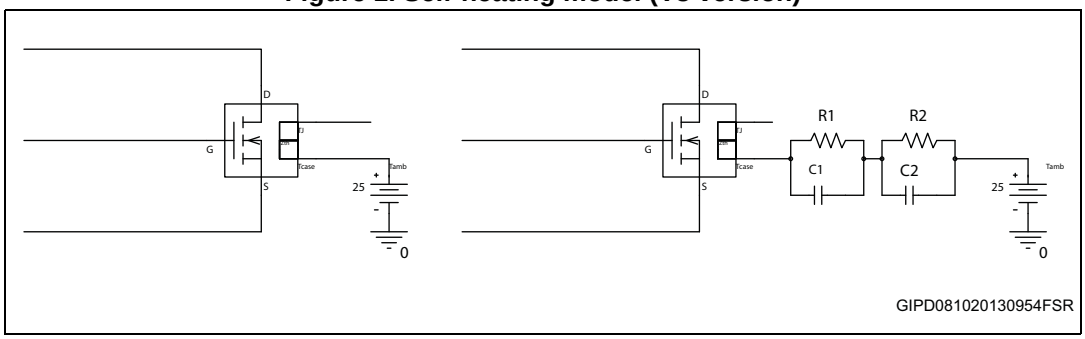
V4 version

It comes directly from V3 version considering the device sited in free air. It includes the package thermal modeling through a thermal equivalent network and presents three additional external thermal nodes: T_j, T_{case} and T_{amb}. The voltage at T_j node and T_{case} node contains all the information about the junction temperature and case temperature which change internal device's parameters. Since they are monitoring nodes, usually T_j and T_{case} pins are not connected (however, to avoid warning messages on this node, the user has to add a floating wire - see *Figure 1*). Conversely, T_{amb} node has to be connected: to a constant voltage source Vdc, representing the ambient temperature.

TN version

It includes the RC thermal network only, which represents the thermal model of the package. Its symbol has two pins: T_j and T_{case}.

Figure 1. Self-heating model (V3 version)

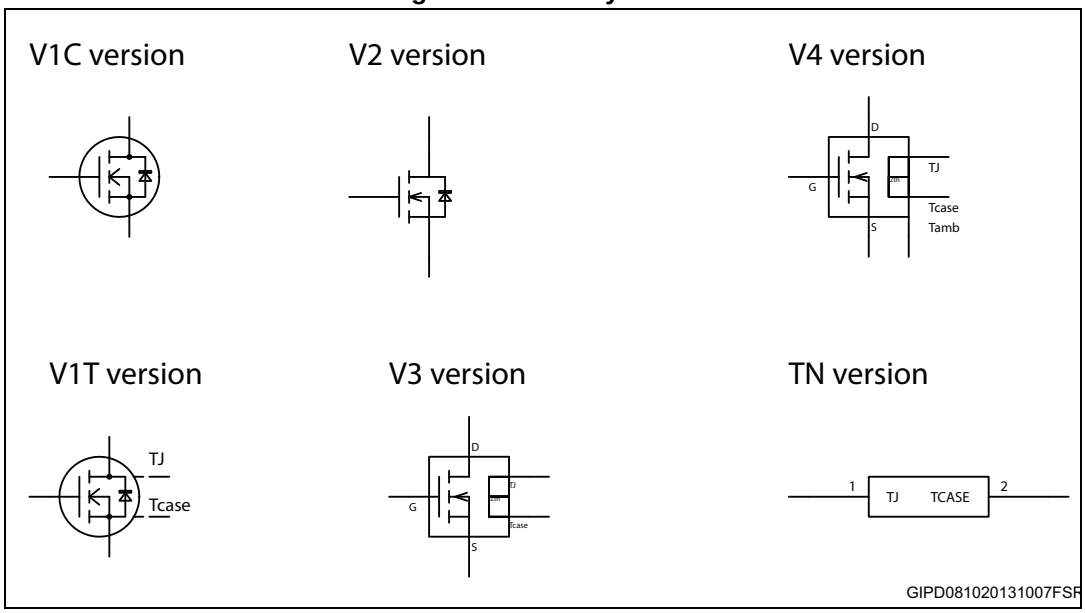


Note: T_j is a monitoring node and it is not connected; T_{case} is connected either by using a Vdc, representing the ambient temperature (on the left-side), or by heat-sink thermal network (on the right-side).

2 Spice model symbol

For each model version, ST provides the appropriate symbol as shown below:

Figure 2. Model symbols



3 Spice models - instructions to simulate

In Spice simulator, user has to upload the device symbol (.OLB file) and the Spice model (.LIB file) to simulate transistors in the schematic.

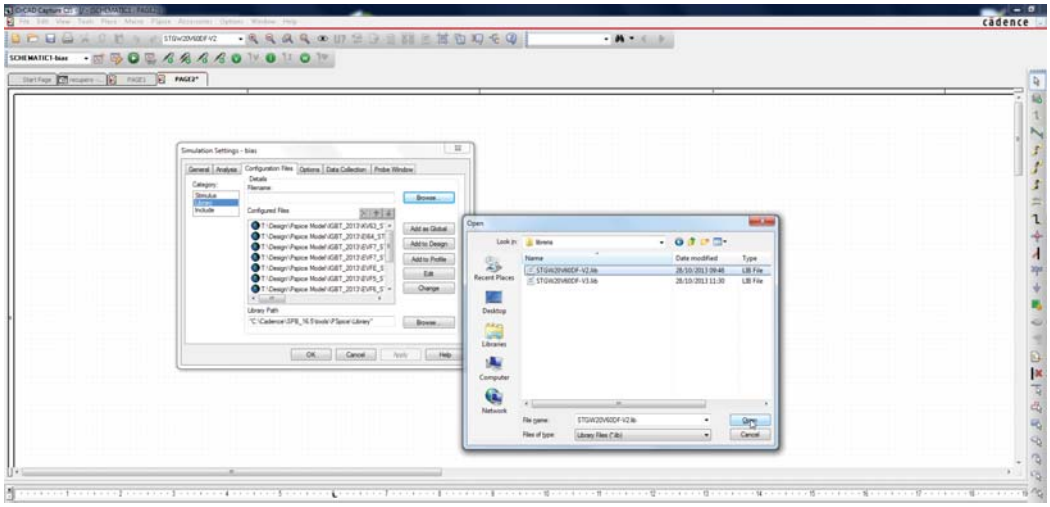
3.1 Installation

In the package model, there are the following files:

- name.lib text file representing the model library written as a Spice code;
- name.olb symbol file to use the model into Orcad capture user interface.

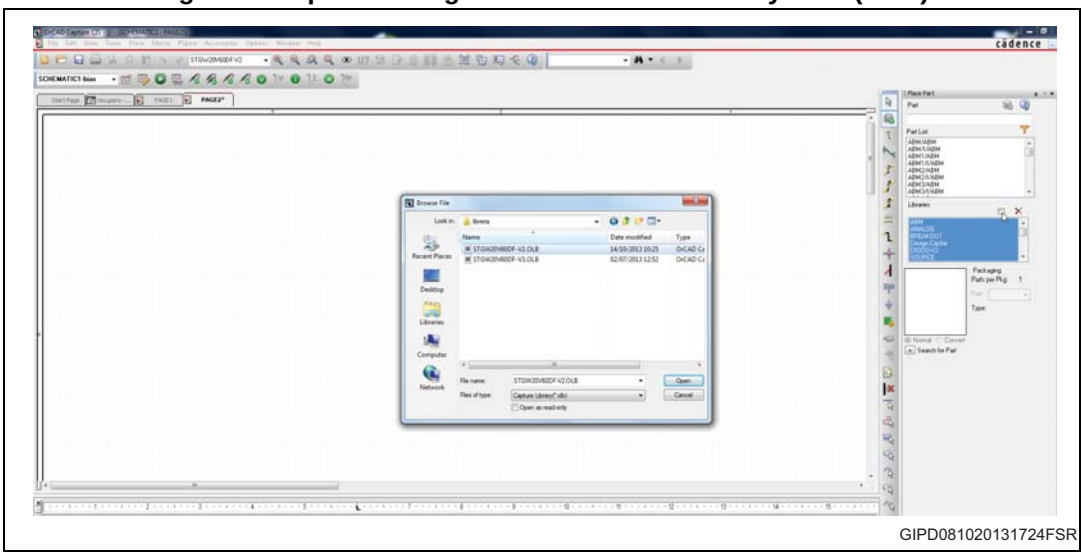
In Capture open the menu dialog window "Pspice" "Edit Simulation Profile". Go to "Configuration Files" tab and "Library" category. Select the library (*.lib) path by "Browse…" button and click to "Add to Design" (see *Figure 3*)

Figure 3. Capture dialog window to select the library (*.lib)



To include the symbol *.olb in the schematic view, open the menu dialog window "Place" "Part" (or simply pressing "P" key in keyboard) and click the "Add Library…" button (or pressing Alt+"A") to select the file (see figure below).

Figure 4. Capture dialog window to include the symbol (*.olb)



Finally, you can simulate your circuit choosing the simulation type and parameters.

3.2 Typical simulation parameters / options

As our models contain many non-linear elements, the standard simulation parameters are often not suitable.

The following values can facilitate convergence (set them in dialog window "Pspice" "Edit Simulation Profile" "Options" tab):

ABSTOL= 1nA	(best accuracy of currents)
CHGTOL= 1 pC..10 pC	(best accuracy of charges)
ITL1= 150	(DC and bias 'blind' iteration limit)
ITL2= 20...150	(DC and bias 'best guess' iteration limit)
ITL4= 20...150	(transient time point iteration limit)
RELTOL= 0.001...0.01	(relative accuracy of voltages and currents)

Note: If the following error message appears during the simulation of one of device models:

==> INTERNAL ERROR -- Overflow in device..... <==

you have to edit the 'PSPICE.INI' file by inserting the following line behind the headline [PSPICE] as follows:

[PSPICE]

MathExceptions = off

.....

DO NOT CHANGE ANY OTHER LINES ALREADY PRESENT

4 A brief description of self-heating model (V3 version)

Power MOSFET's Spice models are behavioral and achieved by fitting simulated data with static and dynamic characterization results.

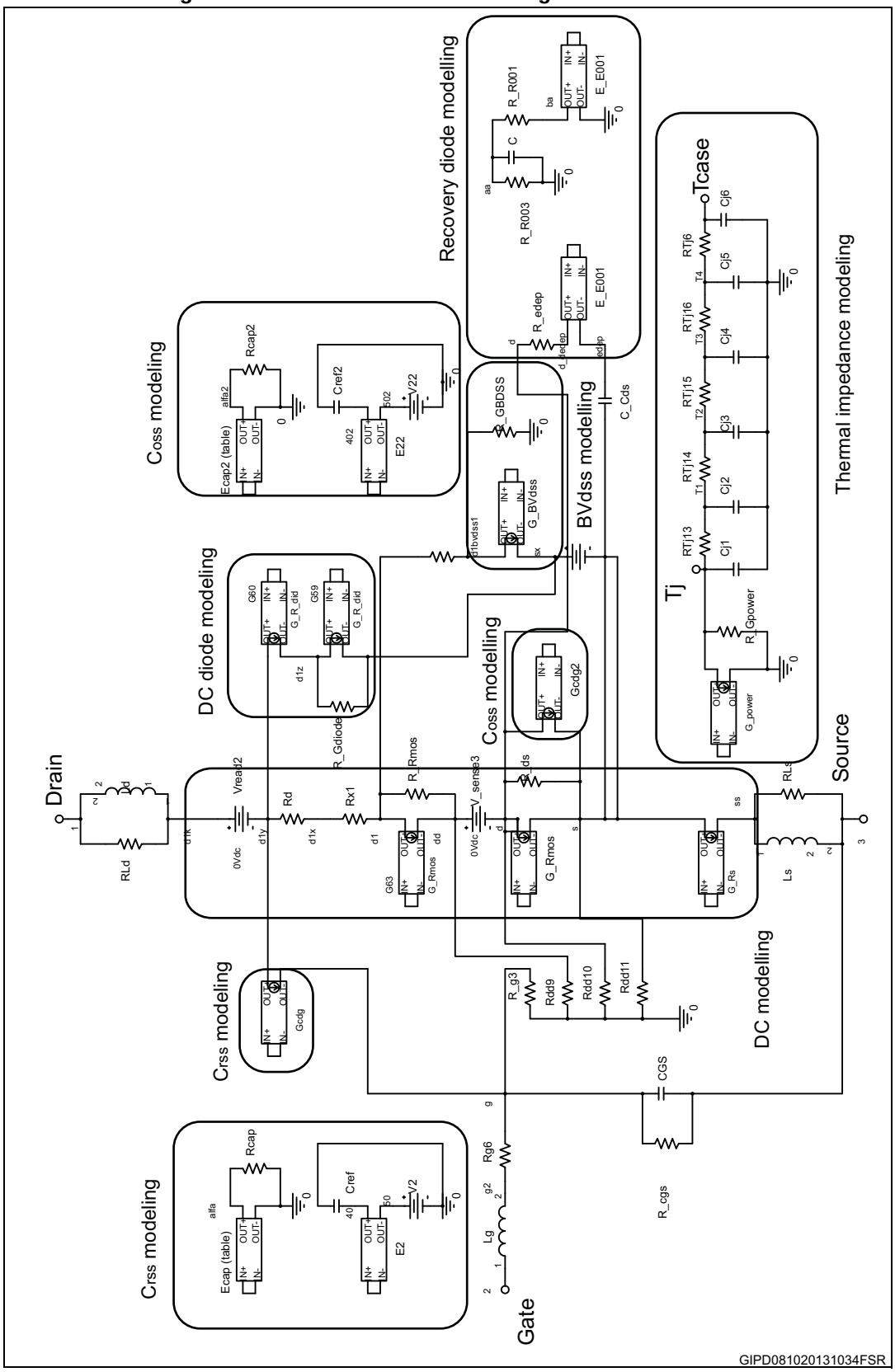
The behavioral model is the best approach because it reproduces the electrical and thermal behavior of the power device through a simplified physical description of the device consisting in a set of equations ruling its behavior at terminal level.

The self-heating model (V3 version) includes different analog behavioral models (ABM) to describe resistors, voltage and current generator, which are temperature-dependent.

A curve fit optimization algorithm extracts the mathematical expression for ABM, which yields a good representation of Power MOSFET's static and dynamic characteristics.

In *Figure 5*, the self-heating spice model (V3 version) schematic is shown.

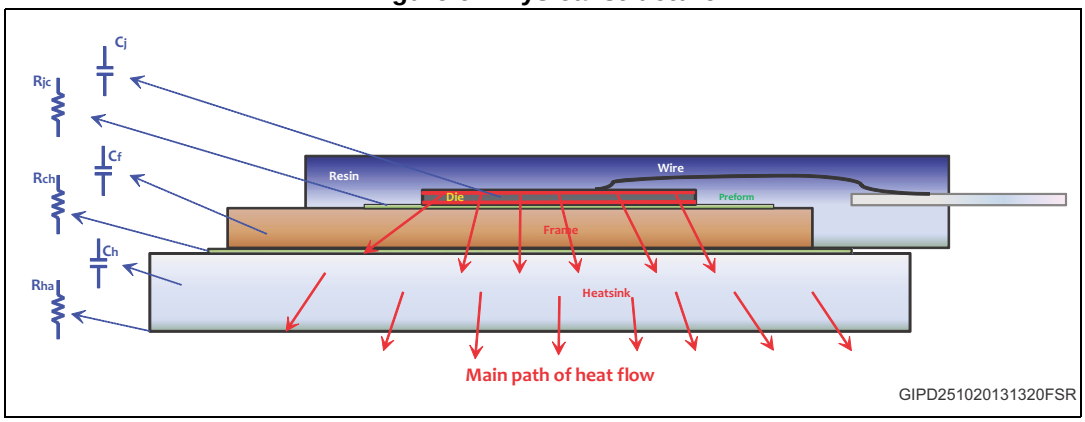
Figure 5. Power MOSFET self-heating model schematic



4.1 Thermal network

Thermal impedance network represents the basic element, which is featured inside the macro-model. It is used to transform the power dissipated inside the junction into a voltage representing the temperature (T_j).

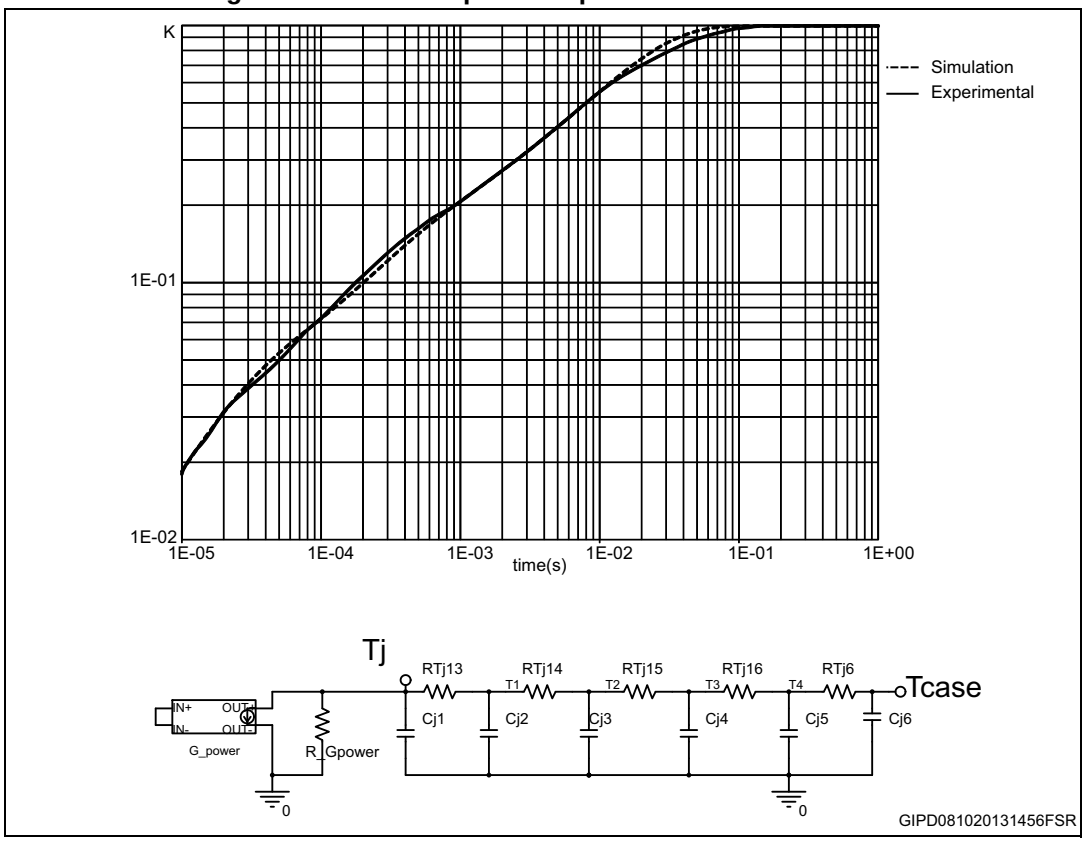
Figure 6. Physical structure



The voltage drop across the network is detected and used as emitter value inside behavioral equations used to model other parameters.

Thermal impedance is the experimental data required to obtain the Cauer model (see *Figure 6*).

Figure 7. Thermal impedance profile and Cauer model



4.2 Experimental data used to fit the model

The model implementation requires the following experimental data:

- Typ. output characteristics at different temperatures
- Typ. transfer characteristics at different temperatures
- Typ. drain source breakdown voltage at different temperatures
- Typ. drain source on state resistance vs temperature
- Typ. gate threshold voltage vs temperature
- Typ. forward diode characteristics
- Typ. capacitances profile vs VDS
- Typ. gate charge
- Typ. switching on resistive load
- Typ. switching on inductive load
- Typ. free-wheeling diode characteristics
- Unclamped inductive switching
- Switching losses vs gate resistance
- Equivalent capacitance time related ($C_{o(tr)}$)
- Equivalent capacitance energy related ($C_{o(er)}$)
- Max. transient thermal impedance

Figure 8. Simulated and measured output characteristics

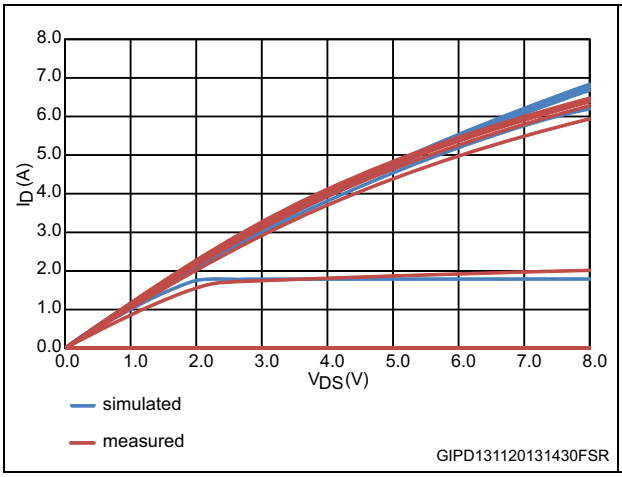


Figure 9. Simulated curves at V_{GS} = 10 V

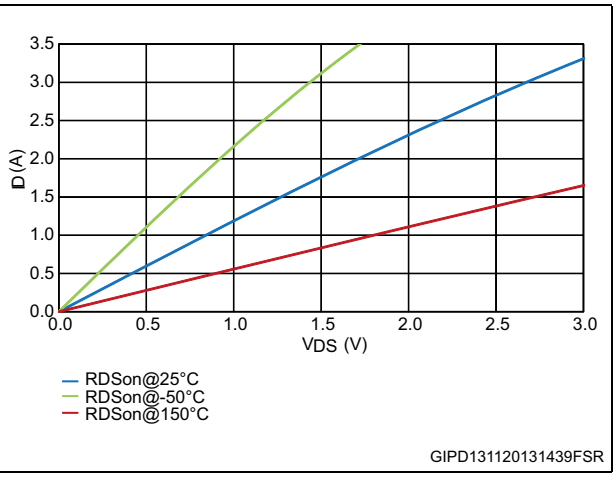


Figure 10. Normalized $R_{DS(on)}$ vs temperature

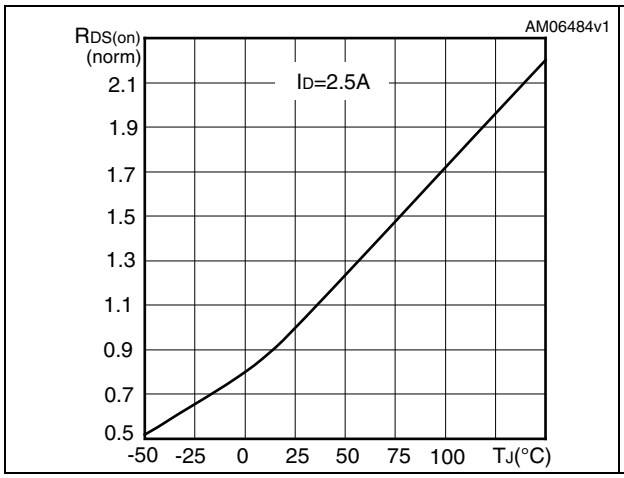
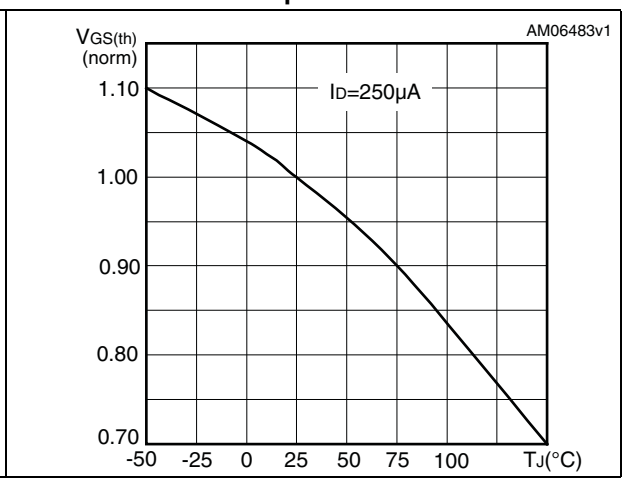


Figure 11. Normalized gate threshold voltage vs temperature



4.3 C_{OSS} and C_{RSS} model

Charge and current formulas for a linear capacitor are:

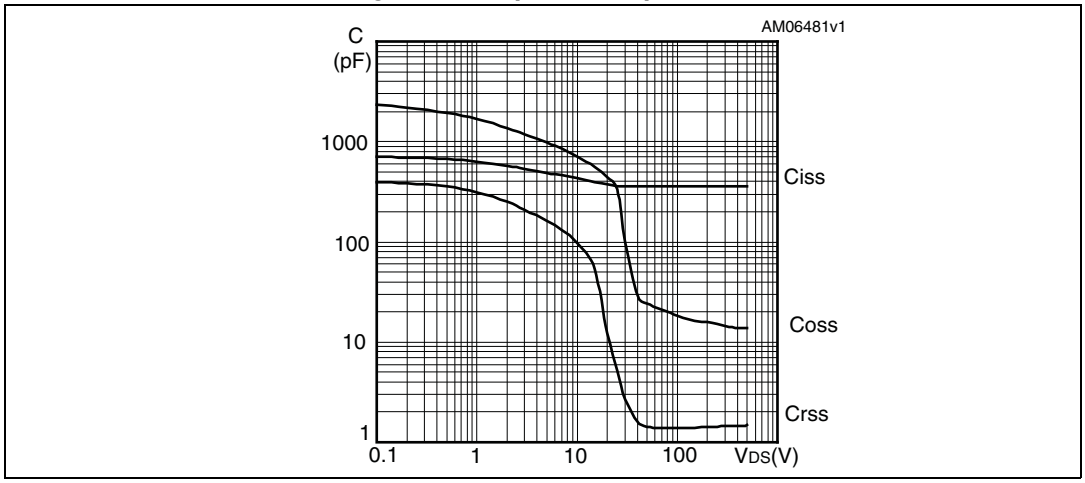
$$Q = C \bullet V \qquad i(t) = C \bullet \frac{dV}{dt}$$

For a non linear (voltage-dependent) time-independent capacitor these formulas become:

$$Q = \int C(V)dV \qquad i(t) = C(V) \bullet \frac{dV}{dt}$$

The C(V) function is obtained by lookup table.

Figure 12. Capacitance profiles



4.4 Example of dynamic characteristics

4.4.1 Gate charge

Figure 13. Gate charge - schematic

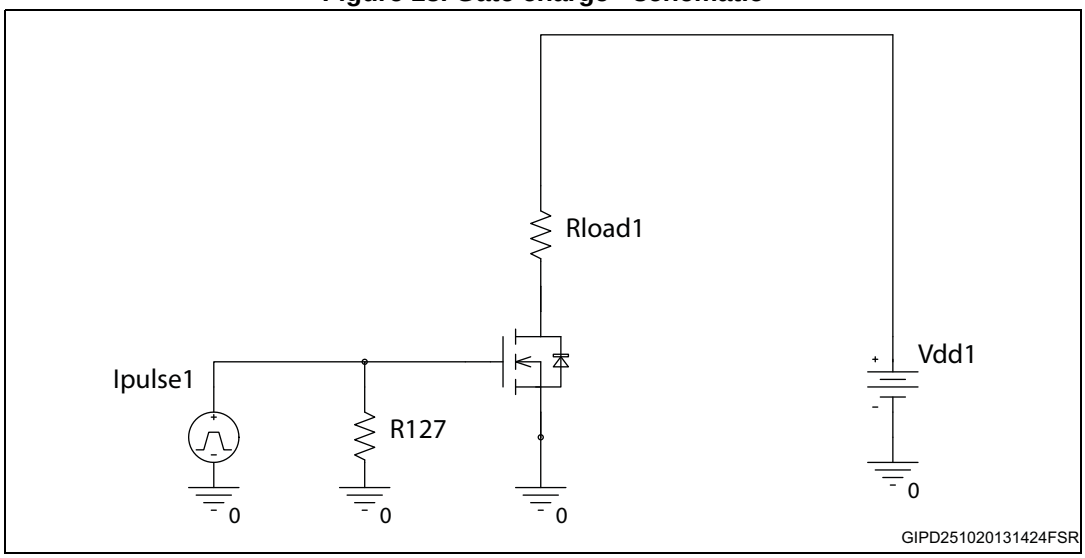


Figure 14. Gate charge - simulated waveforms

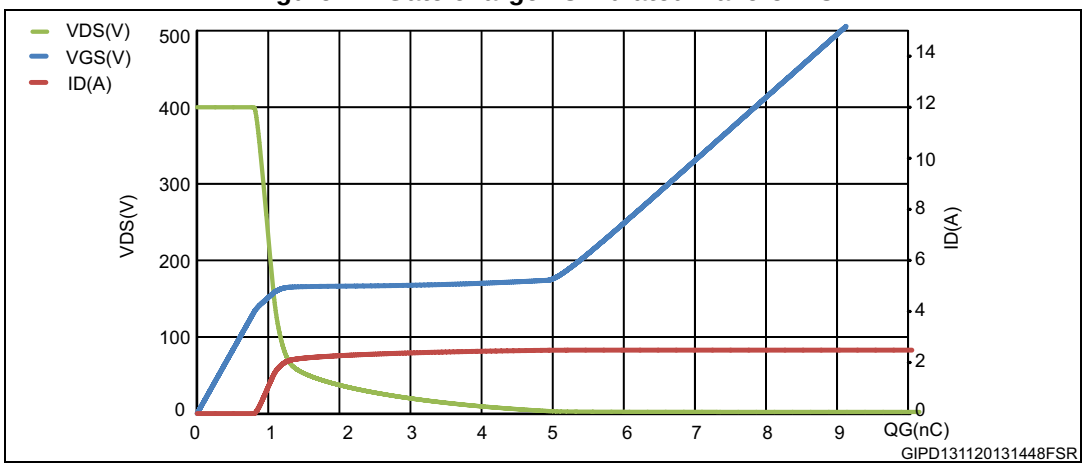
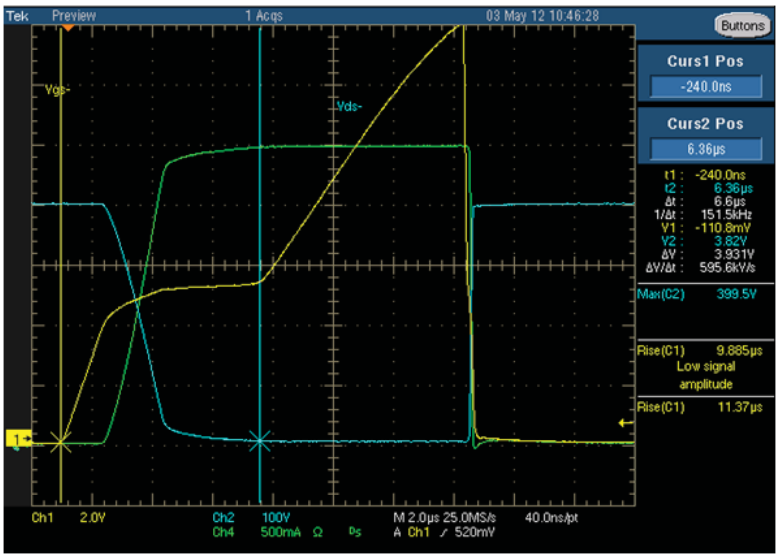


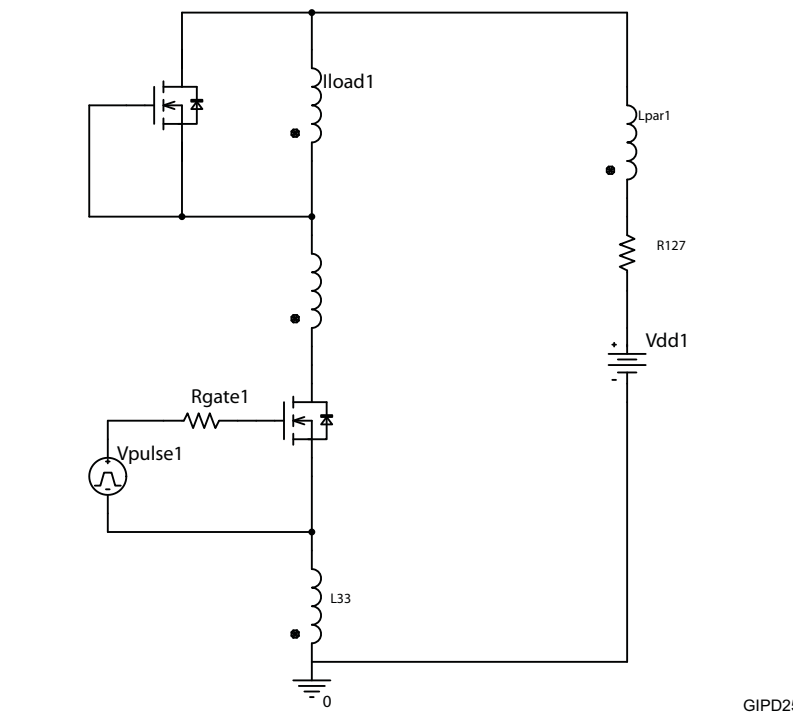
Figure 15. Gate charge - experimental waveforms



GIPD251020131457FSR

4.4.2 Switching on inductive load

Figure 16. Switching on inductive load - schematic



GIPD251020131432FSR

Figure 17. Switching on inductive load - simulated waveforms

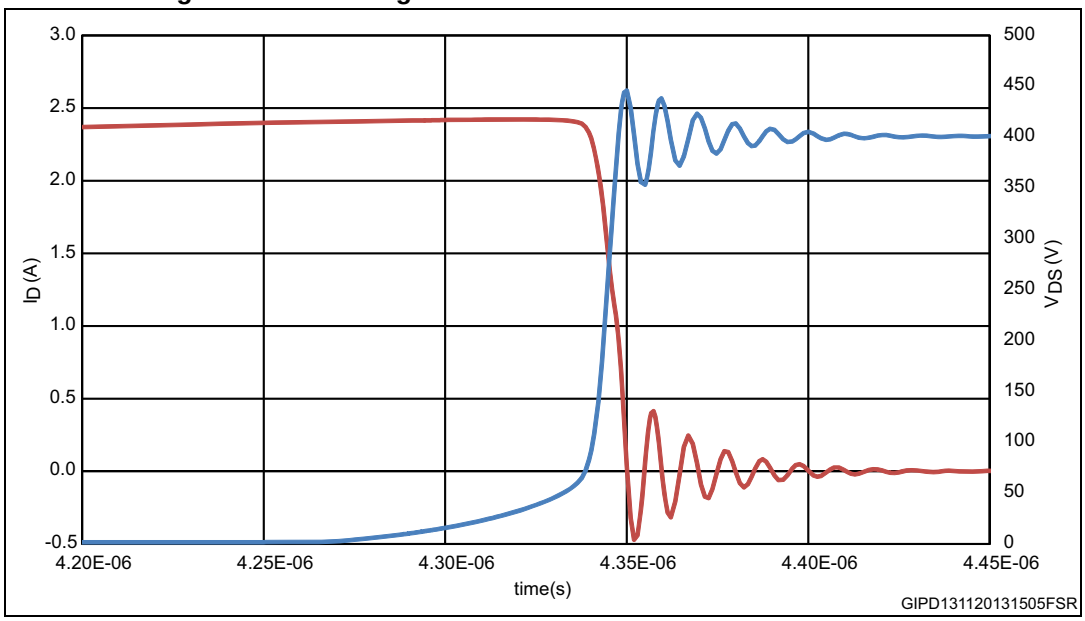
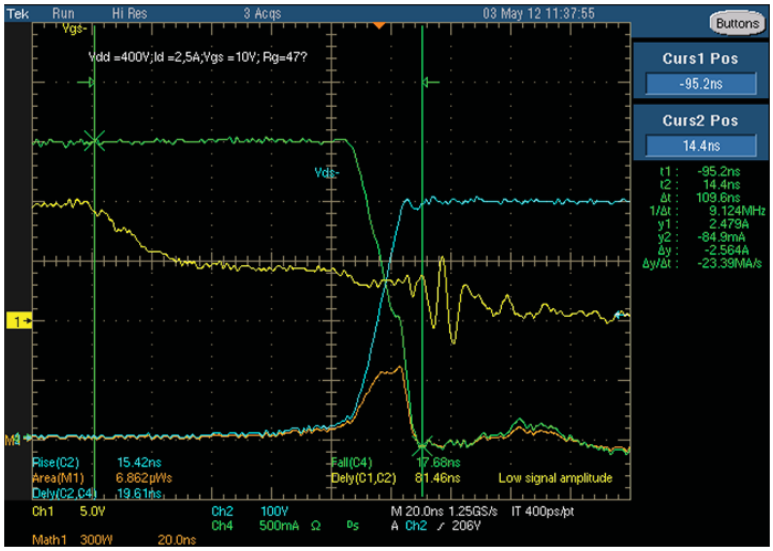


Figure 18. Switching on inductive load - experimental waveforms



4.4.3 E_{off} vs R_{gate}

Figure 19. E_{off} vs R_{gate} - schematic

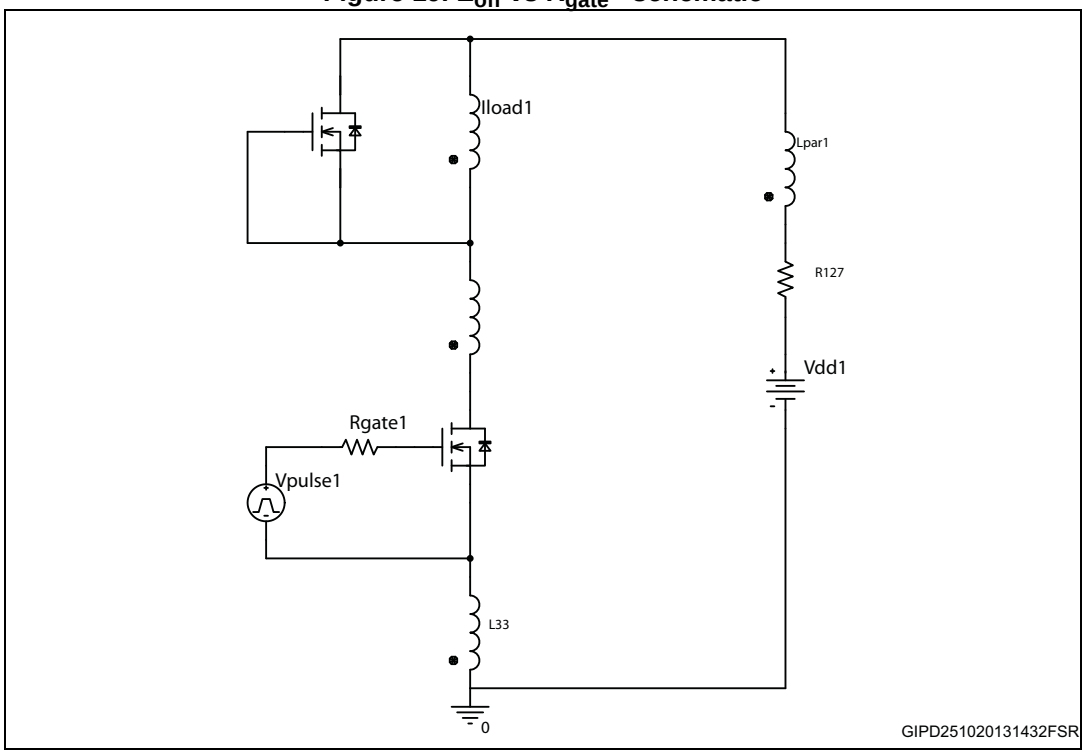


Figure 20. E_{off} vs R_{gate} - experimental waveforms

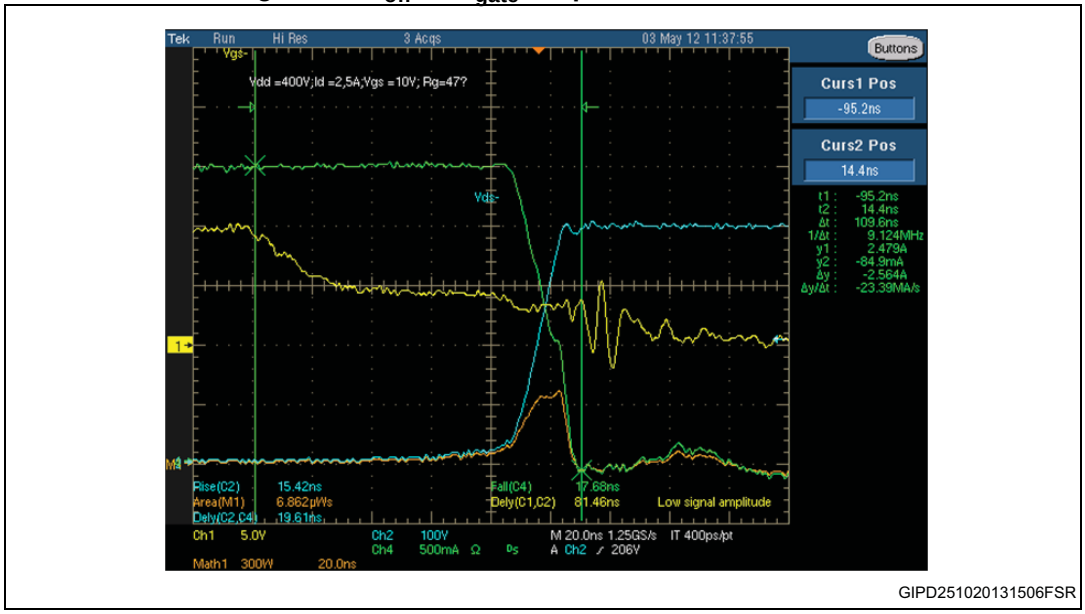


Table 1. E_{off} (comparison simulated/measured)

R_G (Ω)	Measured E_{off} (µJ)	Simulated E_{off} (µJ)
4.7	4.1	3.9
10	4.31	4.4
47	6.8	7.1
200	27	29

4.4.4 Recovery diode

Figure 21. Recovery diode - schematic

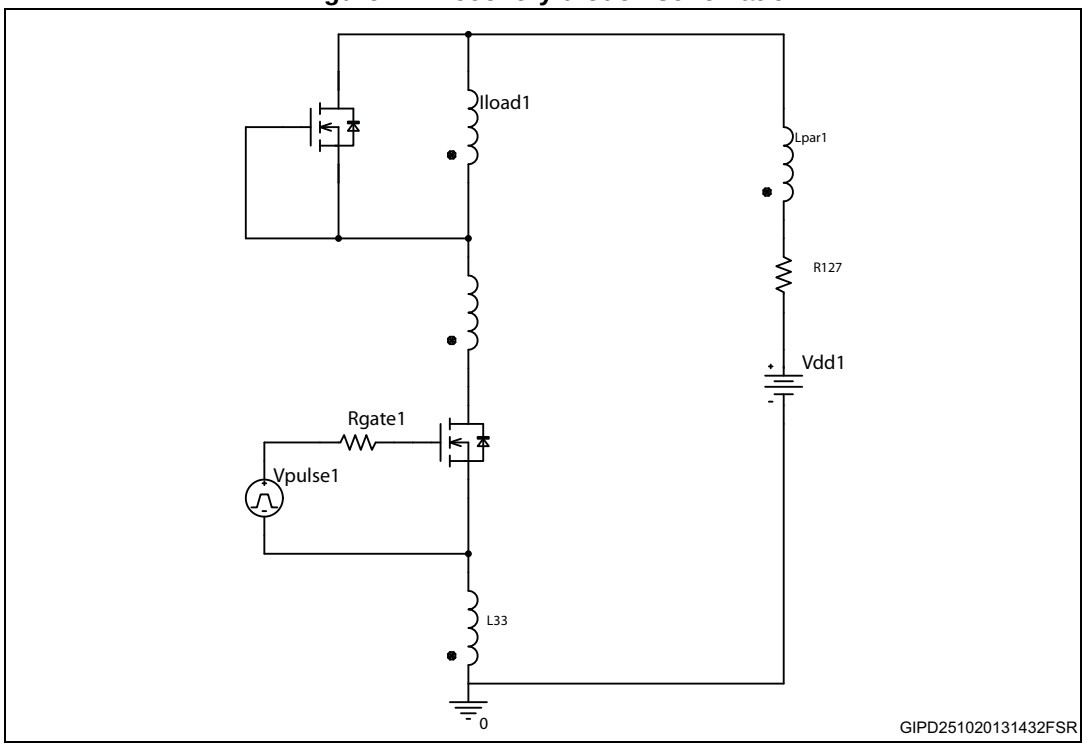
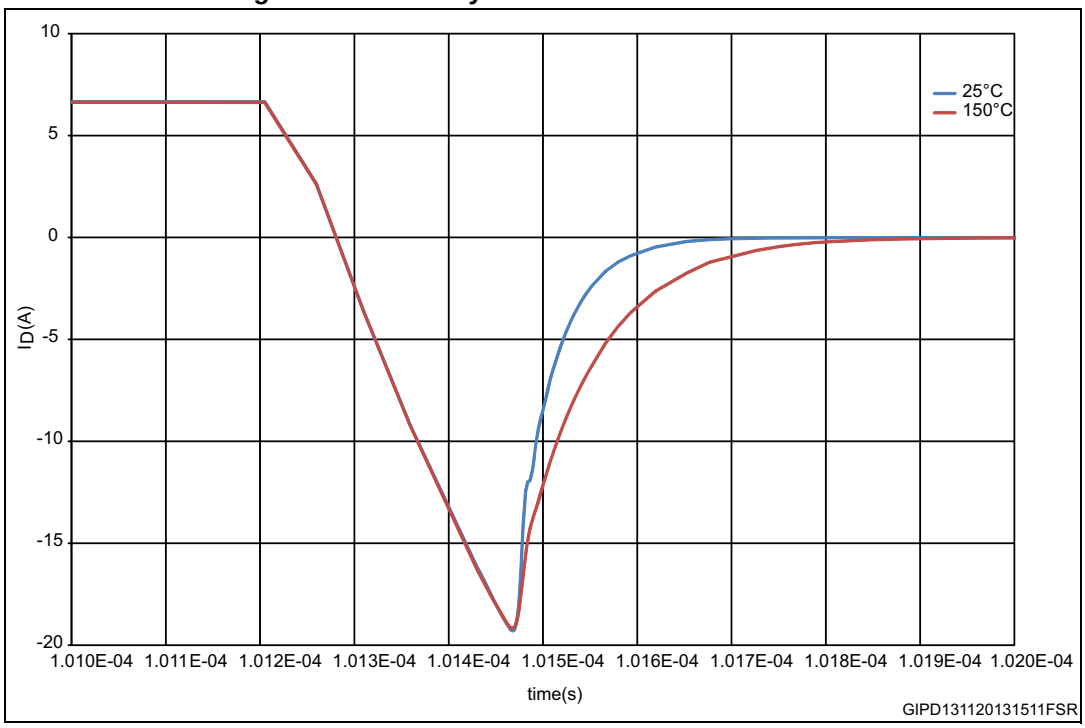


Figure 22. Recovery diode - simulated waveforms



4.4.5 Unclamped inductive switching

Table 2. Simulated test conditions

Test	T_C	Energy	I_{drain}	ΔT_j
1	110 °C	0.3 J	83 A	83 °C
2	110 °C	0.3 J	203 A	133 °C

Figure 23. Unclamped inductive switching - schematic

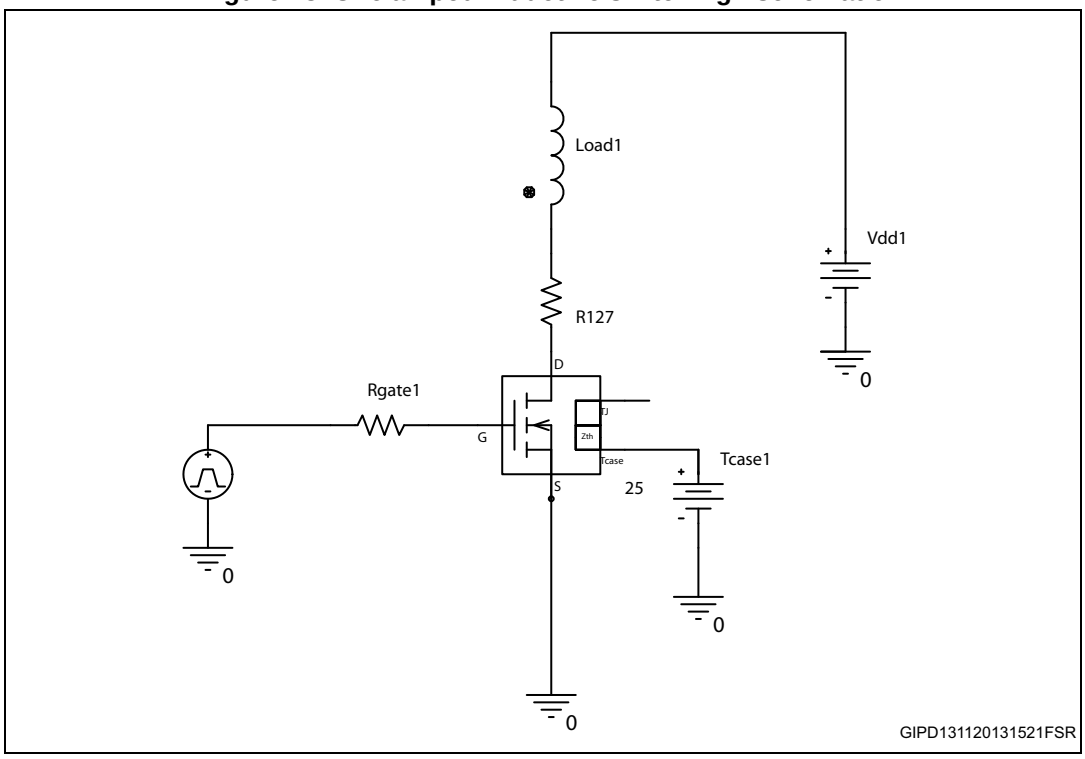


Figure 24. Unclamped inductive switching - simulated waveforms (test 1)

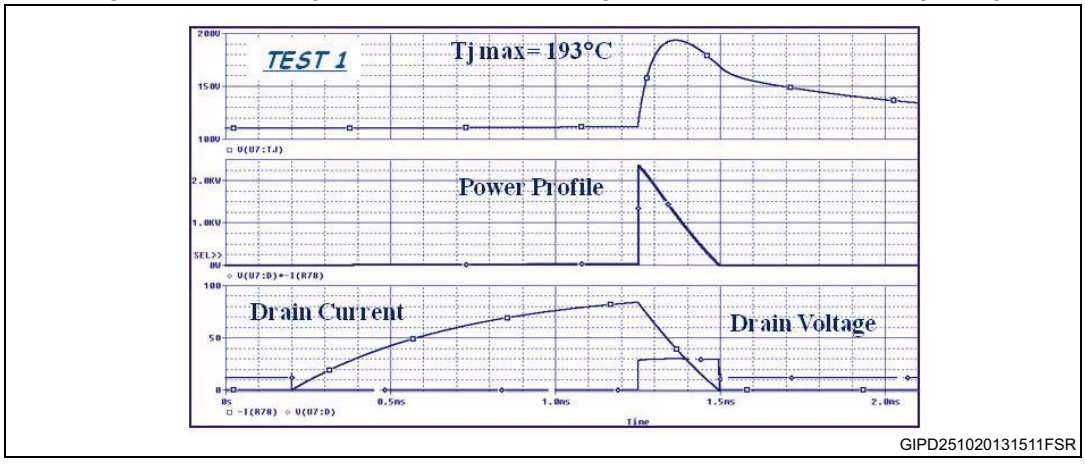


Figure 25. Unclamped inductive switching - simulated waveforms (test 2)

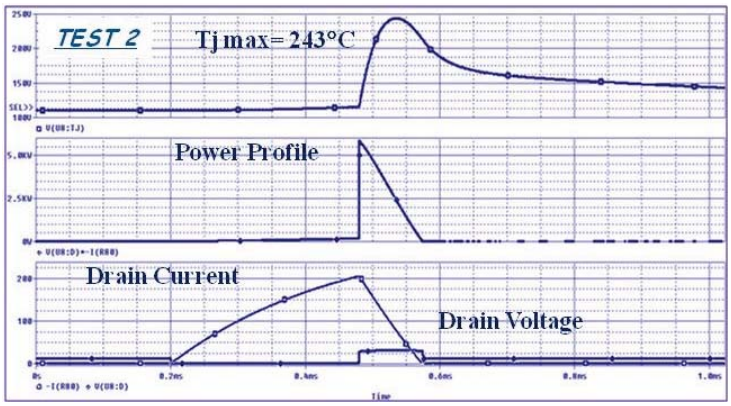


Figure 26. Unclamped inductive switching - experimental waveforms

4.4.6 Short-circuit test

Figure 27. Short-circuit test - schematic

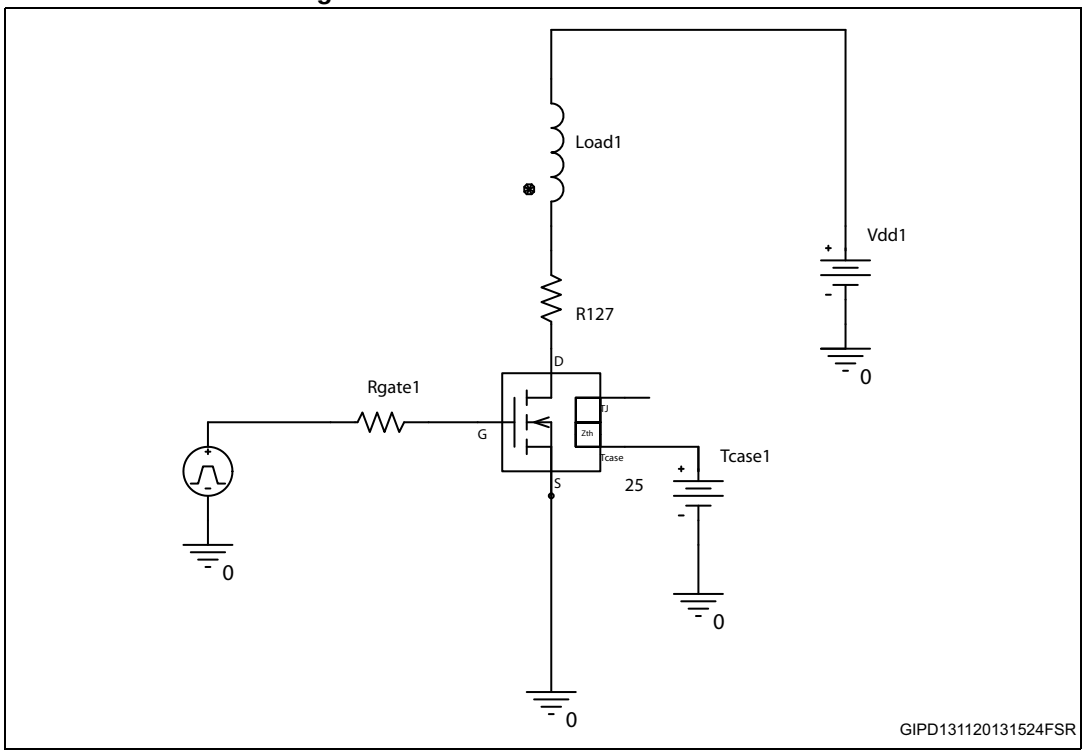
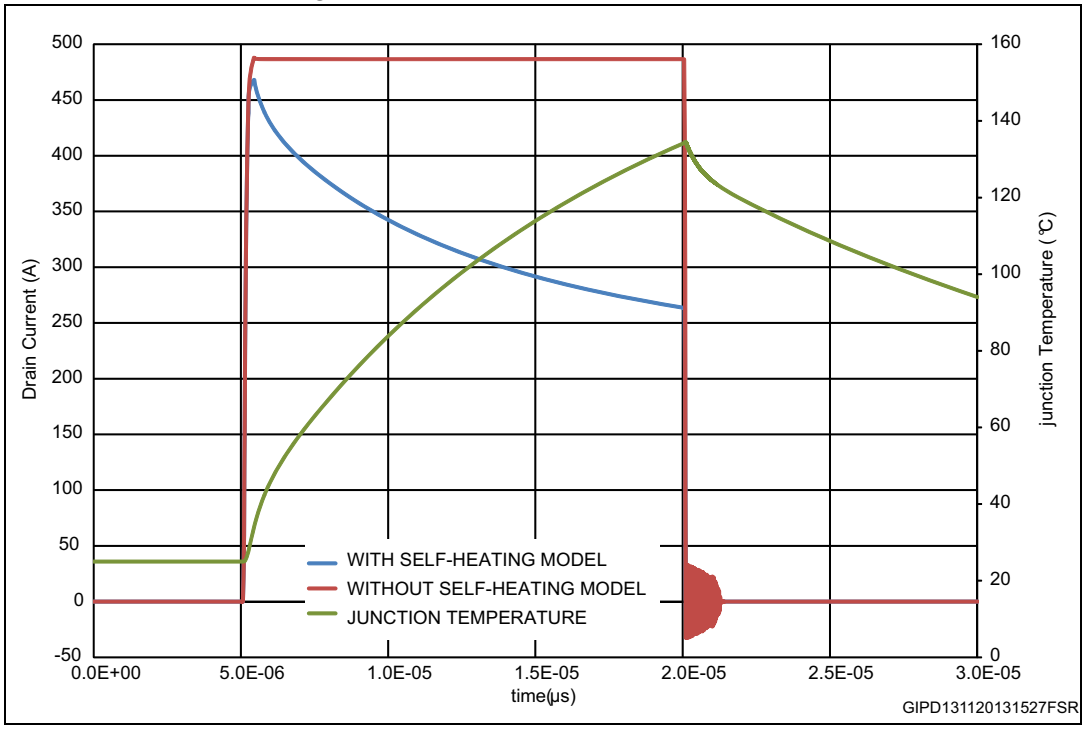


Figure 28. Short-circuit test - waveforms



4.4.7 Flyback simulated by self-heating model

Figure 29. Flyback simulated by self-heating model - schematic

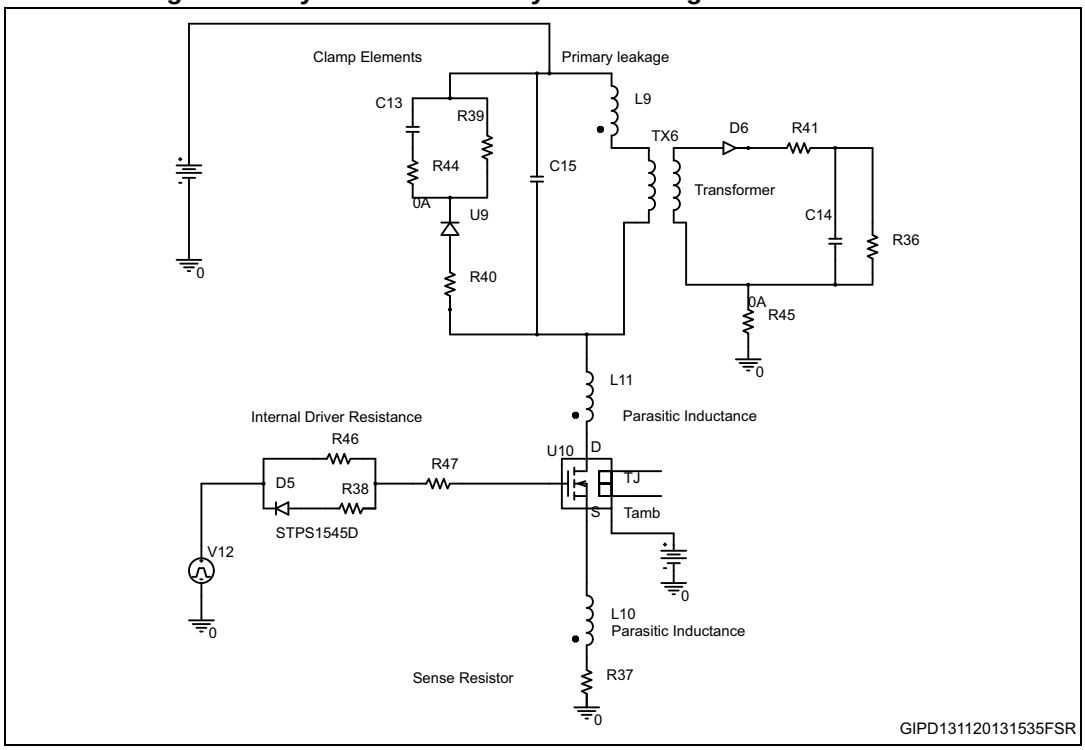
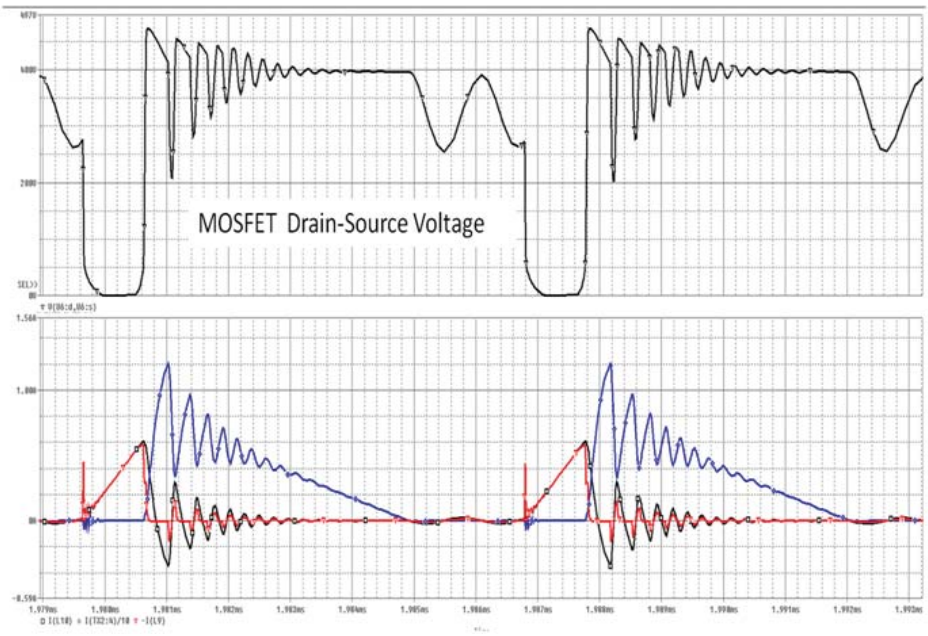


Figure 30. Flyback simulated by self-heating model - simulated waveforms



where:

- Blue line = (Tx current sec)/10
- Black line = (Tx current Pri)
- Red line = MOSFET drain current

If you have further questions, feel free to contact us via our local sale offices.

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
25-Nov-2013	1	Initial release.

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